

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-4 (canceled)

1 **Claim 5 (currently amended):** A semiconductor device,
2 ~~comprising: combining and disposing means for~~ which is
3 formed by combining and disposing pre-registered functional
4 blocks, and ~~wiring means for~~ determining a wiring pattern
5 in accordance with a given logic circuit specification,
6 ~~wherein~~ at least one of the functional blocks ~~has~~
7 comprising:

8 a logic circuit, and,

9 a diode, ~~the diode~~ which is composed of a first
10 conduction type diffusion layer and a second conduction
11 type well connected to a power source, and

12 wherein the diode is connected to a potential-clamped
13 input terminal of the at least one of the functional
14 blocks.

1 **Claim 6 (previously presented):** The semiconductor
2 device as claimed in Claim 5, wherein the logic circuit is
3 a memory.

1 **Claim 7 (previously presented):** A method of designing
2 a semiconductor device, comprising the steps of:
3 combining and disposing pre-registered functional
4 blocks, and
5 determining a wiring pattern in accordance with a
6 given logic circuit specification,
7 wherein at least one of the functional blocks has a
8 logic circuit and a diode,
9 the diode is composed of a first conduction type
10 diffusion layer and a second conduction type well connected
11 to a power source, and
12 the diode is connected to a potential-clamped input
13 terminal of the at least one of the functional blocks.

1 **Claim 8 (previously presented):** A computer-readable
2 recording medium, on which the method of designing a
3 semiconductor device, as claimed in Claim 7, is stored as
4 a program to be executed by a computer.

1 **Claim 9 (previously presented):** A design support
2 apparatus for a semiconductor device, comprising:
3 combining and disposing means for combining and
4 disposing pre-registered functional blocks, and
5 wiring means for determining a wiring pattern in
6 accordance with a given logic circuit specification,

7 wherein at least one of the functional blocks has a
8 logic circuit and a diode, and

9 wherein the diode is composed of a first conduction
10 type diffusion layer and a second conduction type well
11 connected to a potential-clamped input terminal of the at
12 least one of the functional blocks.

1 **Claim 10 (currently amended):** A semiconductor device,
2 ~~comprising: combining and disposing means for combining~~
3 which is formed by combining and disposing pre-registered
4 functional blocks, and

5 ~~wiring means for~~ determining a wiring pattern in
6 accordance with a given logic circuit specification,

7 wherein at least one of the functional blocks has a
8 logic circuit and a diode which is at least connected to an
9 input pin where results of an antenna ratio exceed an
10 allowed antenna ratio,

11 the diode is composed of a first conduction type
12 diffusion layer and a second conduction type well connected
13 to a power source, and

14 the diode is connected to a potential-clamped input
15 terminal of the at least one of the functional blocks.

1 **Claim 11 (previously presented):** The semiconductor
2 device as claimed in Claim 10, wherein the logic circuit is
3 a memory.

1 **Claim 12 (previously presented):** A method of
2 designing a semiconductor device, comprising the steps of:
3 combining and disposing pre-registered functional
4 blocks, and
5 determining a wiring pattern in accordance with a
6 given logic circuit specification,
7 wherein at least one of the functional blocks has a
8 logic circuit and a diode which is at least connected to an
9 input pin where results of an antenna ratio exceed an
10 allowed antenna ratio,
11 wherein the diode is composed of a first conduction
12 type diffusion layer and a second conduction type well
13 connected to a power source, and
14 the diode is connected to a potential-clamped input
15 terminal of the at least one of the functional blocks.

1 **Claim 13 (previously presented):** A computer-readable
2 recording medium, on which the method of designing a
3 semiconductor device, as claimed in Claim 12, is stored as
4 a program to be executed by a computer.

1 **Claim 14 (currently amended):** A design support
2 apparatus for a semiconductor device[[,]] comprising:
3 combining and disposing means for combining and
4 disposing pre-registered functional blocks, and

5 wiring means for determining a wiring pattern in
6 accordance with a given logic circuit specification,
7 wherein at least one of the functional blocks has a
8 logic circuit and a diode which is at least connected to an
9 input pin where results of an antenna ratio exceed an
10 allowed antenna ratio, and
11 wherein the diode is composed of a first conduction
12 type diffusion layer and a second conduction type well
13 connected to a potential-clamped input terminal of the at
14 least one of the functional blocks.

1 **Claim 15 (previously presented):** The semiconductor
2 device as claimed in Claim 5, wherein the diode is
3 connected to a port between an output of the logic circuit
4 and the input terminal of the functional block.

1 **Claim 16 (new):** A semiconductor device comprising at
2 least one functional block having a logic circuit and a
3 diode composed of a first conduction type diffusion layer
4 and a second conduction type well connected to a power
5 source, wherein the diode is connected to a potential-
6 clamped input terminal of the at least one functional
7 block.

1 **Claim 17 (new):** The semiconductor device as claimed
2 in Claim 16, wherein the logic circuit is a memory.

1 **Claim 18 (new):** The semiconductor device as claimed
2 in Claim 16, wherein the diode is connected to a port
3 between an output of the logic circuit and the input
4 terminal of the functional block.

1 **Claim 19 (new):** A semiconductor device comprising at
2 least one functional block having a logic circuit and a
3 diode which is at least connected to an input pin where
4 results of an antenna ratio exceed an allowed antenna
5 ratio, wherein the diode is composed of a first conduction
6 type diffusion layer and a second conduction type well.
7 connected to a power source and wherein the diode is
8 connected to a potential-clamped input terminal of the at
9 least one of the functional blocks.

1 **Claim 20 (new):** The semiconductor device as claimed
2 in Claim 19, wherein the logic circuit is a memory.